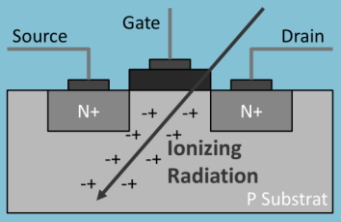
SEU-TID-Core

Detector-IP for Single Event Upsets and Aging



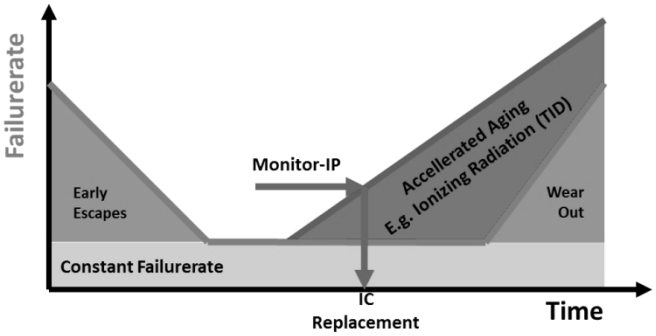
Detector-IP for Single Event Upsets / Aging Effects (Total Ionizing Dose)

Features:

- Error detection to validate SEU (Single Event Upsets) occurrences
- In Situ Monitoring of aging effects according TID (Total Ionizing Dose)
- Process, voltage and temperature (PVT) independent TID measure-ments
- Inspection of the functionality for Risk Based Maintenance
- Determination of remaining useful life (RUL)
- Customized control interface, easily adaptable for standard interfaces (e.g. JTAG, AHB)
- Fault Insertion (FI) features for SEU and TID

Applications:

- Embedded systems, control systems, signal processing and data storage in high radiation environments (e.g. medical equipment, aviation, aerospace, nuclear power plant)
- Robust design and test methodology for use in critical radiation environments for digital integrated circuits (ASIC, FPGA, ASSP)



Targeted Devices:

- Actel/Microsemi Family
- Others supported upon request

Core Deliverables:

- Encrypted VHDL Soft Core
- Test Bench

Synthesis/Simulation Support:

- Simulation: ModelSim®
- Synthesis: Synplicity®
- Other tools supported upon request

Verification Support:

- Test Bench
- Test Vectors

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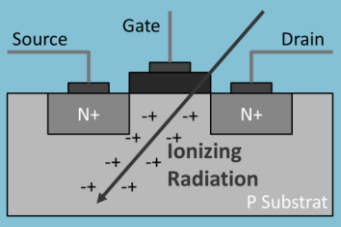

Description:

The configurable IP-Core is designed to detect radiation effects in high energetic radiation environments. It is able to detect soft errors, monitors aging effects and covers the following features:

- Error Detection Flag (EDF)
- Error Detection Output (EDO)
- Error Detection Counter (EDC)
- Delay Chain Output (DCO)
- DCO counters (DCO0, DCO1)

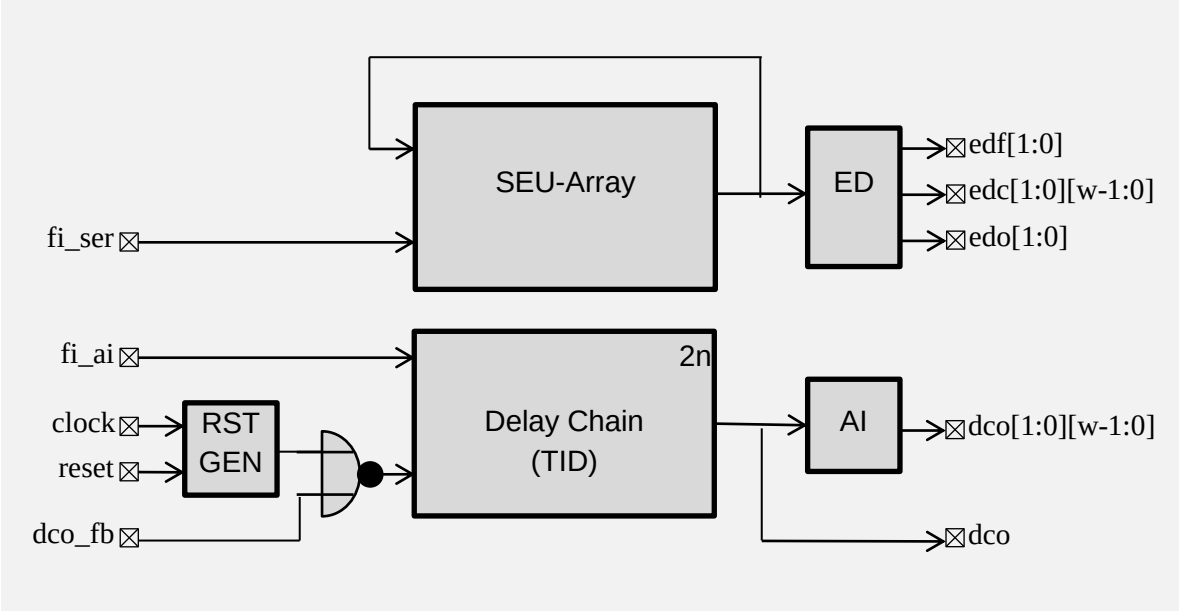

Figure 1 Principle Architecture

The architecture comprises a configurable detector array (SEU). Error information (flags, counters, location) is sampled and stored on-chip and can be accessed by a customized interface for offline analysis.

Aging effect monitoring can be done by means of a configurable delay chain (DC). The aging index (AI) unit performs frequency measurements and PVT independent continuous variance analysis.

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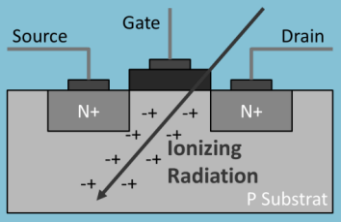

Functional Description

Reset Generator (RSTGEN)

The configurable reset generator converts the asynchronous reset signal into a synchronous reset. It initializes the ring oscillator and resets the flipflops.

SEU-Array

The configurable SEU array creates the pattern signature for SEU detection. It is a 2- dimensional array with length n. It stores the resulting signature after SEU events. Fault injection is possible by the input FI_SER.

Error Detection (ED) Unit

The ED unit evaluates the signature of the SEU-Array. Error flags are generated after SEU events. The number of events is stored in the ED counters (EDC). The signature itself is serially available at ports EDO.

Delay Chain (TID)

There is a configurable delay chain implemented with length 2n. The non-inverting output of the delay chain is external available at port DCO and is fed back to the dco_fb input forming a ring oscillator which is initialized by the RSTGEN block. Real HW fault insertion is possible in the delay chain when synthesized with the generic variable g_fi_ai_hw active. In this case the fault insertion itself is controlled by the signal fi_ai.

Unit AI (aging index)

In situ monitoring of aging effects according TID (Total Ionizing Dose) by means of inspection of the delay chain and ring oscillator offers Risk Based Maintenance by intelligent frequency measurement and continuous variance analysis without the need to memorize the initial value of the frequency. Furthermore the realization is independent of temperature and voltage variations of the supply voltage. Thus no calibration is necessary. The results are available at the counter outputs DCO[1:0][w-1:0].

Implementation possibilities

The functionality can be implemented as standalone Diagnosis Device (FPGA) embedded on system boards or embedded as IP-core in system chips (ASIC, SOC, ASSP).

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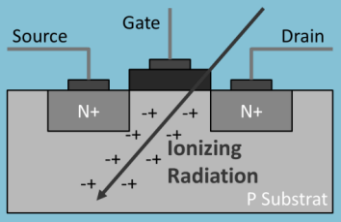

Signal Descriptions

The following signal descriptions define the IO signals.

Signal	Direction	Description
clock	input	Clock for the IP block (e.g. 166 or 200 MHz)
reset	input	Asynchronous reset signal (high active)
fi_seu	input	Fault insertion for single event upsets (SEU)
fl_ai	input	Fault insertion for the aging index
dco_fb	input	Feedback input of the DCO output
edf[1:0]	output	Error detection flags
edo[1:0]	output	Error detection outputs (localisation signature)
edc[1:0][w-1:0]	output	Error detection counters
dco	output	Delay chain output
dco[1:0][w-1:0]	output	DCO counters (aging index)

Description of the Generics

The following table defines the generic variables.

Generic	HW/SIM affected	Description
g_fi_ai_hw	HW	HW fault insertion (AI)
g_n	HW	Delay chain length (2n, even)
g_rstc	HW	Reset clock cycles
g_countw	HW	Counter width (w)
g_td	SIM	Basic delay
g_x, g_y	SIM	Simulation factors

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